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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Applicant Number	09/759,414		
		Filing Date	01-13-2001		
		First Named Inventor	LI, ZHE		
		Group Art Unit	2123		
		Examiner Name	TESKA, KEVIN J.		
Sheet	1	of	2	Attorney Docket Number	

Tom Stevens

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
THS		S.-Y. HUANG et al, "AutoFix: a hybrid tool for automatic logic rectification" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 9, September 1999, pp. 1376-1384, IEEE, U.S.A.	
THS		S.-Y. HUANG and K.-T. CHENG, "ErrorTracer: design error diagnosis based on fault simulation techniques" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 9, September 1999, pp. 1341-1352.	
THS		C.-C. LIN et al, "Logic synthesis for engineering change" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 3, March 1999, pp. 282-292, IEEE, U.S.A.	
THS		S.-Y. HUANG et al, "Fault simulation based design error diagnosis for sequential circuits" Proceedings Design Automation Conference, June 1998, pp. 632-637, ACM, U.S.A.	
THS		A. G. VENERIS and I.N. HAJJ, "A fast algorithm for locating and correcting simple design errors in VLSI digital circuits" Proceedings Great Lake Symposium on VLSI Design, March 1997, pp. 45-50, IEEE, U.S.A.	
THS		S.-Y. HUANG et al, "Incremental logic rectification" Proceedings VLSI Test Symposium, April 1997, pp. 143-149, IEEE, U.S.A.	
THS		S.-Y. HUANG et al, "ErrorTracer: a fault simulation-based approach to design error diagnosis" Proceedings International Test Conference, November 1997, pp. 974-981, IEEE, U.S.A.	
THS		C.-C. LIN et al, "Logic synthesis for engineering change" Proceedings Design Automation Conference, June 1995, pp. 647-652, ACM, U.S.A.	
THS		I. POMERANZ and S. REDDY, "On correction of multiple design errors" IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 2, February 1995, pp. 255-264, IEEE U.S.A.	
THS		I. POMERANZ and S. M. REDDY, "On error correction in macro-based circuits" Proceedings International Conference on Computer-Aided Design, November 1994, pp. 568-574, ACM, U.S.A.	
THS		D. BRAND et al, "Incremental synthesis" Proceedings International Conference on Computer-Aided Design, November 1994, pp. 14-18, ACM, U.S.A.	

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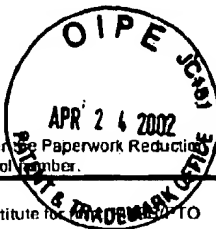
Examiner Signature	<i>Tom Stevens</i>	Date Considered	5/20/04
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THS		A. KUEHLMANN et al, "Error diagnosis for transistor-level verification" Proceedings Design Automation Conference, June 1994, pp. 218-224, ACM, U.S.A.	
THS		I. POMERANZ and S.M. REDDY, "A method for diagnosing implementations errors in synchronous sequential circuits and its implications on synthesis" Proceedings European Conference on Design Automation, September 1993, pp. 252-258, IEEE.	
THS		M. FUJITA, "Methods for automatic design error correction in sequential circuits" Proceedings European Conference on Design Automation, September 1993, pp. 76-80, IEEE.	
THS		P.-Y. CHUNG et al, "Diagnosis and correction of logic design errors in digital circuits" Proceedings Design Automation Conference, June 1993, pp. 503-508, IEEE, U.S.A.	
THS		S.-Y. KUO, "Locating logic design errors via test generation and don't-care propagation" Proceedings European Design Automation Conference, September 1992, pp. 466-471, IEEE.	
THS		P.-Y. CHUNG and I.N. HAJJ, "ACCORD: automatic catching and correction of logic design errors in combinational circuits" Proceedings International Test Conference, October 1992, pp. 742-751, IEEE, U.S.A.	
THS		Y. WATANABE and R. BRAYTON, "Incremental synthesis for engineering changes" Proceedings International Conference on Computer-Aided Design, November 1991, pp. 40-43, IEEE, U.S.A.	
THS		M. TOMITA et al, "An algorithm for locating logic design errors" Proceedings International Conference on Computer-Aided Design, November 1990, pp. 468-471, IEEE, U.S.A.	
THS		H.-T. LIAW et al, "Efficient automatic diagnosis of digital circuits" Proceedings International Conference on Computer-Aided Design, November 1990, pp. 464-467, IEEE, U.S.A.	
THS		J.C. MADRE et al, "Automating the diagnosis and the rectification of design errors with PRIAM" Proceedings International Conference on Computer-Aided Design, November 1989, pp. 30-33, IEEE, U.S.A.	
THS		K.A. TAMURA, "Locating functional errors in logic circuits" Proceedings Design Automation Conference, June 1989, pp. 185-191, ACM, U.S.A.	

Examiner Signature	Date Considered
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